UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SYNOPSYS, INC.,

Plaintiff,

v.

SIEMENS INDUSTRY SOFTWARE INC.,

Defendant.

Case No. 20-cv-04151-WHO

CLAIM CONSTRUCTION ORDER

Re: Dkt. No. 101, 113, 114

In this matter, plaintiff Synopsys, Inc. ("Synopsys") asserts infringement claims against defendant Siemens Industry Software Inc. ("Siemens"). The parties request construction of ten terms from four patents asserted by Synopsys, all of which relate to semiconductor technology. My constructions are below.

BACKGROUND

Synopsys and Siemens are competitors in the field of semiconductor technology. On June 23, 2020, Synopsys filed this action against Avatar Integrated Systems, Inc. ("Avatar"), alleging that Avatar's Aprisa and Apogee products infringed several Synopsys patents. *See* Dkt. No. 1. On July 6, 2020, Synopsys filed a corrected complaint. *See* Dkt. No. 9. On December 1, 2020, Avatar merged into Siemens and ceased to exist as a standalone entity. *See* Dkt. No. 51. The parties subsequently stipulated to substitute Siemens as defendant for Avatar. *See* Dkt. Nos. 58, 59. Synopsys accuses Siemens of infringing one or more claims of four of its patents: U.S. Patent No. 7,546,567 ("the '567 Patent"); U.S. Patent No. 7,853,915 ("the '915 Patent"); U.S. Patent No. 8,234,614 ("the '614 Patent"); and U.S. Patent No. 8,407,655 ("the '655 Patent"). I held a claim construction hearing on June 25, 2021 ("Claim Construction Hearing"). Dkt. No. 126.

LEGAL STANDARD

Claim construction is a matter of law. *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "Generally, a claim term is given its ordinary and customary meaning—the meaning that a term would have to a person of ordinary skill in the art in question at the time of the invention." *Howmedica Osteonics Corp. v. Zimmer, Inc.*, 822 F.3d 1312, 1320 (Fed. Cir. 2016) (internal quotation marks and citation omitted). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Such redefinition or disavowal need not be express to be clear. *Trustees of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1364 (Fed. Cir. 2016).

In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005); *see also Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998) ("The appropriate starting point . . . is always with the language of the asserted claim itself."). Like a person of ordinary skill in the art, courts read terms in the context of the claim and of the entire patent, including the specification. *Phillips*, 415 F.3d at 1313. The specification is "the single best guide to the meaning of a disputed term." *Vitronics*, 90 F.3d at 1582. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998).

"A claim is invalid for indefiniteness if its language, when read in light of the specification and the prosecution history, fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1377 (Fed. Cir. 2015) (citation and internal quotation marks omitted). It is "legal error" for a court to instruct a jury to give a claim term its "plain and ordinary" meaning when there are unresolved

disputes as to a claim's scope. *Eon Corp. IP Holdings LLC v. Silver Spring Networks, Inc.*, 815 F.3d 1314, 1318 (Fed. Cir. 2016).

In most situations, analysis of this intrinsic evidence alone will resolve claim construction disputes, *Vitronics*, 90 F.3d at 1583; however, a court can further consult "trustworthy extrinsic evidence" to compare its construction to "widely held understandings in the pertinent technical field," *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999). Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). All extrinsic evidence should be evaluated in light of the intrinsic evidence, *Phillips*, 415 F.3d at 1319, and courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernible from examination of the claims, the written description, and the prosecution history, *Pitney Bowes*, 182 F.3d at 1308 (citing *Vitronics*, 90 F.3d at 1583).

DISCUSSION

I. '567 PATENT

The '567 Patent is titled "Method and Apparatus for Generating a Variation-Tolerant Clock-Tree for an Integrated Circuit Chip." Dkt. No. 1-1, Ex. 3 ("'567 Patent"). The invention relates to techniques for generating a clock tree on an integrated circuit ("IC") chip to facilitate reducing the effects of on-chip variation ("OCV"). *Id.* at 1:11–13. Components in ICs are generally synchronized by a clock signal, whose frequency governs the speed of the circuit. *Id.* at 1:23–29. In such circuits, a clock distribution network—or "clock tree"—is used to distribute the clock signal from a common source to various circuit components, such as a register. *Id.*

Claim 1 of the '567 Patent recites,

> "A method for generating a clock-tree on an integrated circuit (IC) chip, comprising:
> receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout;
> generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers; and

> clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers, wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other;
> wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs."

'567 Patent at 10:55–11:7. Independent claim 13 is similar but relates to "[a] computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method for generating a clock-tree on an integrated circuit (IC) chip, the method comprising" the steps above. *Id.* at 12:6–28. Independent claim 25 recites,

> "A computer system that generates a clock-tree on an integrated circuit (IC) chip, comprising:
> a processor;
> a memory;
> a receiving mechanism configured to receive a placement for a chip layout, where the placement includes a set of registers in fixed locations in the chip layout:
> a generating mechanism configured to generate a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers; and
> a clustering mechanism configured to cluster the set of registers based on the timing criticality profile to create a clock-tree for the set of registers, wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other;
> wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs."

Id. at 14:4–25.

A. "timing criticalities between pairs of registers"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"timing criticality between a pair of registers"	value derived from the data path delay between a pair of registers connected by a data path	a value computed from an estimate of 'timing slack' for a pair of registers and their data path, such that a lower slack means a higher timing criticality	value derived from the data path delay between a pair of registers connected by a data path

		With or without the above constructions: Indefinite.	

The ’567 Patent teaches clustering pairs of registers based on their timing criticalities. Dkt. No. 113 at 3. A “register” is a circuit component made up of logic gates that temporarily stores data until the arrival of a clock signal and synchronizes the data. Dkt. No. 119 (“Synopsys Technology Tutorial”). A clock signal travels along a “data path” from a launcher register to a capturer register. ’567 Patent at 5:57–59. “Timing criticality” relates to the risk that the clock signal will arrive late. *Id.* at 5:40–42. A “timing slack” is the margin between an arrival time of a clock signal at a capturer register and the required time for the circuit to operate correctly. The parties agree that “timing slack” is calculated from “the value equal to the clock period minus the sum of the setup time of the capturer, the clock skew, and the data path delay.” *Id.* at 5:57–67, 7:4–13; Dkt. No. 102, Joint Claim Construction and Prehearing Statement (“JCCS”) at 5:11–15. A “negative slack” means the clock signal is expected to arrive late. ’567 Patent at 5:65–67; Dkt. No. 119. The parties agree that a “data path delay” is the “time required for a data signal at the output of the launcher to reach the input of the capturer” register. JCCS at 1.

1. Indefiniteness

Siemens argues that the claim term “timing criticality” is indefinite because (1) there are multiple meanings of “timing criticality”; and (2) “timing criticality” is only an estimate during the pre-routing stage and therefore the patent does not outline clear boundaries for an artisan to avoid practicing the claim element. Dkt. No. 114 at 4–7.

According to Siemens, the term “timing criticality” was accepted as a general concept in 2007, when the ’567 Patent was filed, but was known to have different meanings. Dkt. No. 114 at 6; Dkt. No. 113-6 (“Robins Rep.”) ¶ 47. Siemens also points to the internal inconsistencies within the patent itself. For example, the patent defines “timing criticality” as depending on “timing slack.” *See* ’567 Patent at 8:59–9:12 (“the highest priority register pair (i.e., the one with the worst timing slack)”). Dependent claim 2 also recites that “obtaining the timing criticality between a pair of registers . . . involves computing a timing slack between the pair of registers.”

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Id. at 11:8–11. At the same time, the patent gives an example in which a register pair is given a higher timing criticality value "if [it] has a longer data path delay." '567 Patent at 7:19–24. Consequently, Siemens argues that these internal inconsistencies suggest that the term "timing criticality" is indefinite. Dkt. No. 114 at 6.

The term is sufficiently definite. Both parties agree that the '567 Patent describes "timing criticality" as a function of either "data path delay" or "timing slack." Dkt. No. 118 at 2; *see Eli Lilly & Co. v. Teva Parenteral Meds., Inc.*, 845 F.3d 1357, 1371 (Fed. Cir. 2017) (holding that a term was sufficiently definite even though the written description of the patent used the term in two different ways). Both parties' experts agree that the two concepts are related: timing slack is calculated from data path delay. JCCS at 5 (citing '567 Patent at 5:59–67) (defining "timing slack" as the clock period minus the sum of the setup time of the capturer, the clock skew, and the data path delay); Dkt. No. 113-2 ("Friedman Rep.") ¶ 28; Robins Rep. ¶ 51. A person having ordinary skill in the arts ("POSITA") would therefore see no internal contradictions within the patent. *See Barbaro Techs., LLC v. Niantic, Inc.*, No. 18-CV-02955-RS, 2020 WL 6749367, at *3 (N.D. Cal. Feb 12, 2020) (holding that the term was not indefinite in part because the various explanations of the term were "not necessarily inconsistent.").

Siemens also argues that the term "timing criticality" is imprecise because at the pre-routing stage, it can only be predicted and so the patent provides "no objective boundaries for determining what types of calculations for a pair of registers are not predictions of 'timing criticality.'" Dkt. No. 114 at 7. Synopsys responds that an exact value is not necessary and so Siemens's objection is inapposite. Dkt. No. 113 at 5. Skilled artisans would understand that "timing criticality" is to be derived using estimates, such as the estimated net length, which is then used to estimate path delay in early stages of circuit design. *Id.* As Synopsys points out, Siemens's argument would render "all patents directed at pre-routing stages of the circuit design process . . . invalid as all calculations necessarily involve estimates." Dkt. No. 118 at 3. I conclude that the term "timing criticality" is sufficiently definite.

2. Proposed Constructions

The question then is which proposal is the proper construction. Siemens argues that its

construction—which indicates that "timing criticality" is computed from an estimate of timing slack—is better than Synopsys's construction for four reasons. Dkt. No. 114 at 4. First, the patent defines "timing criticality" as depending on "timing slack." *See* '567 Patent at 8:59–9:12 ("the highest priority register pair (i.e., the one with the worst timing slack)"). Second, the patent states that "a timing criticality can be computed based on the slack" and outlines the formula for calculating slack from four parameters on which the parties agree. *Id.* at 7:5–9; *see* JCCS at 5. Third, both parties' experts agree that timing slack is one art-recognized meaning of "timing criticality" between registers. Robins Rep. ¶ 47; Friedman Rep. ¶ 34. Finally, a delay in data signal is logically more closely tied to slack than path delay. Dkt. No. 114 at 4. Siemens argues that Synopsys's construction is uncertain in part because data path delay is only one out of four parameters that affect "timing criticality" whereas its construction identifies all four parameters—clock period, set up time of the capturer, clock skew, and data path delay. Dkt. No. 114 at 4.

Synopsys opposes Siemens's alternate construction because it introduces two improper limitations: (1) "limiting the term to values derived from timing slack rather than data path delay"; and (2) "requiring it to be inversely related to slack." Dkt. No. 113 at 5. According to Synopsys, limiting the term to values derived from "timing slack" would render the dependent claims superfluous in violation of the claim differentiation doctrine. "[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005). Dependent claim 2 states, "The method of claim 1, *wherein obtaining the timing criticality* between a pair of registers in the set of registers *involves computing a timing slack* between the pair of registers based on the received placement." *See* '567 Patent at 11:8–11 (emphasis added).

Siemens responds that its construction would not render dependent claim 2 superfluous because "claim 2 is narrower" in that "it requires 'computing' timing slack whereas claim 1 encompasses simply receiving already computed timing slack values." Dkt. No. 114 at 6 n.5. Synopsys contests that dependent claim 2 is about obtaining timing criticality as well as computing timing slack and that therefore claims 1 and 2 are "essentially swallowed into each

other as a result of [Siemens's] construction." Dkt. No. 126 at 12.

I agree with Synopsys. As the Federal Circuit held, "where the limitation that is sought to be 'read into' an independent claim already appears in a dependent claim, the doctrine of claim differentiation is at its strongest." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). As Synopsys's expert also points out, the patent describes dependent claim 2 as a variation on the embodiment described in claim 1. *See* '567 Patent at 2:26–29 ("In a variation on this embodiment, the process obtains the timing criticality between a pair of registers by computing a timing slack between the pair of registers based on the received placement."). As a result, the doctrine of claim differentiation undermines Siemens's argument that "timing criticality" is derived from an estimate of timing slack.

Synopsys also asserts that Siemens's construction improperly excludes a key embodiment. Dkt. No. 118 at 4; Dkt. No. 126 at 9–10. The patent recites an embodiment where timing criticality is derived from data path delay alone:

> "[A]n edge between each pair of launcher/capturer is assigned a weight (for example, from 0 to 10) based on its timing criticality. For example, in FIG. 3, the edge between register pair 304/306 will be assigned a higher weight than the edge between register pair 314/316 if the former has a longer data path delay. In order to reduce the complexity of the timing graph G, only those edges associated with sufficiently large weights will be included in the graph, and considered as timing critical."

'567 Patent at 7:15–27. Siemens does not explain how its proposal encompasses this embodiment and only responds that this embodiment is an example of why the patent is indefinite, an argument that I rejected above. Dkt. No. 114 at 6; Dkt. No. 126 at 10–11.

In contrast, Synopsys points out that its construction does not eliminate the other embodiments, i.e., the ones that explicitly define timing criticality as related to timing slack, because all timing criticalities must start with or include the data path delay. Dkt. No. 126 at 9. In other words, a timing criticality can be derived by "data path delay alone or it can be more than the data path delay," e.g., "data path delay plus skew plus input plus setup time," which "add up to timing slack." *Id.* at 9–10. Accordingly, although both proposals capture parts of the definition for "timing criticality," Synopsys's construction adopts a more accurate definition by referring to

"data path delay" instead of "timing slack."[1]

B. "on-chip variations"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"on-chip variations"	process and environmental variations that occur within a chip boundary	process and environmental variations that occur within a chip boundary	process and environmental variations that occur within a chip boundary

The parties agree on the construction for "on-chip variations."

C. "registers [at / in] fixed locations"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"registers [at /in] fixed locations"	registers [at/in] a location that is fixed during a phase of the clock tree synthesis	registers at specified locations that are retained in the generated clock-tree If not construed as proposed: Indefinite.	registers [at/in] a location that is fixed during clock-tree generation

The dispute here is (1) whether the term is indefinite without Siemens's construction; and (2) whether the register locations are retained in the generated clock tree or fixed for a phase of the clock tree synthesis. The parties agree that "a clock tree" is "a clock signal distribution network, on a chip, in which there is only one path from a common clock source to any register or clock buffer." JCCMS at 1.

1. Indefiniteness

Siemens contends that the term "fixed location" is indefinite without the limitations of its construction because it does not set clear boundaries for the claim element. Dkt. No. 114 at 9. According to Siemens's expert, Dr. Gabriel Robins, there are multiple meanings of Synopsys's construction: (1) "the location is fixed but one can still move registers from one fixed location to

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[1] Synopsys also argues that Siemens's proposal improperly requires the term to be inversely related to slack because it excludes systems where the timing criticality would be directly, not inversely, proportional to timing slack. Dkt. No. 113 at 5–6. Because I adopt Synopsys's construction, I will not address this argument.

other fixed locations as needed"; (2) "the register is locked into that position now and forever"; or (3) "the register cannot be moved for the duration of clock tree synthesis, but perhaps some downstream optimization would later be allowed to move that register." Robins Rep. ¶ 85.

Synopsys responds that a patentee does not have to define every word in the claim, especially where its meaning would be evident to those in the art. Dkt. No. 113 at 8. According to its expert, a POSITA would understand that the third definition above applies: "the registers are in fixed locations during the clock tree generation stage of clock tree synthesis." Friedman Rep. ¶ 52. Friedman opines that a POSITA would "understand that the '567 Patent only describes the clock tree generation stage and does not address the types of clock tree optimizations that would follow the clock tree synthesis process described in the '567 patent." *Id.* ¶ 52. He explains that the clock-tree generation stage is distinct from post-processing steps of clock-tree synthesis, such as optimization during which the registers can be moved. *See id.* ¶¶ 52–55.

Similarly, Siemens's expert also opines that a POSITA would expect that the location of the registers may change during optimization. Robins Rep. ¶ 82. Robins first describes how the electron design automation ("EDA") processes "can involve many iterations and refinements." *Id.* ¶ 76. For example, even if the verification step of the EDA process succeeds, "it is very common to still perform changes to the design in order to affect optimizations that could further improve some aspect of the chip's design, manufacturability, performance, or reliability somewhere downstream." *Id.* He explains that "A skilled artisan would expect a placement to provide the locations of all the registers, but they would also know that there are many engineering stages in the EDA process. This person would recognize that usually a location currently specified in the placement might be subject to change later, due to potential additional design iterations as described above." *Id.* ¶ 82.

Further, Synopsys's expert points to the specification to explain that the location of the registers does not change. The patent describes a clustering process where "because the location of the registers being clustered together does not change, the bounding box of the clusters has to be modified to include all of the registers within that cluster." Friedman Rep. ¶ 53 (citing '567 Patent at 9:16–41). In addition, one embodiment "makes clear that any changes made to the

placement during the location-based clustering process are discarded." *Id.* ¶ 54 (citing '567 Patent at 8:29–33) ("When the constraints in the set of clusters have been extracted, the process restores the original placement by removing all the clusters and discarding the temporary partial-clock-tree."). Accordingly, the specification and expert testimony indicate that the term is sufficiently definite—a POSITA would understand with reasonable certainty that the location of the registers do not change during clock-tree generation but may change during post-processing optimization. *See* Friedman Rep. ¶ 52; Robins Rep. ¶ 82.

2. Proposed Constructions

Synopsys opposes Siemens's construction to the extent that it requires registers to not change during the entire circuit design process, including optimization. Dkt. No. 113 at 7. I agree. It points out that Siemens's expert does not espouse Siemens's construction. Dkt. No. 118 at 5–6. Instead, Siemens's expert agrees with Synopsys that the location of the registers may change during a later stage in the EDA process, for example, during optimization. Robins Rep. ¶¶76, 82. Synopsys also asserts that Siemens's construction would improperly turn the patent into a product claim rather than a method claim, where the focus is on the generated clock tree instead of the method to generate the clock tree. Dkt. No. 126 at 19.

Siemens contends that my tentative construction—"registers [at/in] a location that is fixed during the clock-tree generation stage"[2]—is problematic because the patent does not use the phrase "clock tree generation stage." Dkt. No. 126 at 15. Instead, where the patent does discuss "stages" it expressly indicates that its embodiments can be used during one or more of the EDA software stages. *Id.*; *see* '567 Patent at 4:64–66. To avoid confusion about the meaning of "stage," I will not use it in the final construction. *See* Dkt. No. 122. Instead, I will construe the term as follows: "registers [at/in] a location that is fixed during clock-tree generation." As explained above, the specification supports the construction that the location of registers are fixed during clock-tree generation. *See* '567 Patent at 8:29–33, 9:16–41. Although Siemens is correct

[2] During the Claim Construction Hearing, Synopsys's counsel agreed with my tentative construction even though it differed from its original construction. Dk. No. 126 at 18.

that the intrinsic evidence does not support moving the registers after clock-tree generation, Dkt. No. 114 at 8, both experts testify that a POSITA would understand that the registers may change during optimization after clock-tree generation. Friedman Rep. ¶ 52, Robins Rep. ¶ 82. Siemens's construction would contradict this understanding; I adopt the construction above.

II. '614 PATENT

The '614 Patent is titled, "Multi-Threaded Global Routing." Dkt. No. 1-1, Ex. 5 ("'614 Patent"). The advancement of semiconductor chips has led to increased complexity in translating from the design to the actual chip layout. *Id.* at 1:11–16. Previously, computers spent considerable time routing wires one at a time, following a single-threading process. '614 Patent at 1:15–16. A thread is defined as "a sequential stream of program code instructions and processing resources used to process the instructions." *Id.* at 1:18–21. The '614 Patent introduces a technique of multi-threaded global routing that executes parallel routing of multiple threads, reducing overall routing time. *Id.* at 1:17–18, 22–23.

Claim 1 of the '614 Patent recites,

> "A method of routing a semiconductor chip's global nets, comprising:
> ranking said semiconductor chip's global nets, wherein
> said ranking includes at least one of the following:
> ranking power/ground nets over clock signal nets;
> ranking power/ground nets over timing/slew critical nets;
> ranking clock signal nets over timing/slew critical nets;
> ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;
> identifying a subset of said global nets;
> routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subsets other global nets;
> identifying a second subset of said global nets;
> routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subsets other global nets but in respect of the routes of said subset of global nets.

Id. at 9:52–9:5. Independent claims 12 and 16 are similar but refer to "[a] non transitory machine readable storage medium having program code stored thereon that when executed by a machine causes a method to be performed" and "[a] computing system having a machine readable storage medium with program code stored thereon that when executed by said computing system's processing resources cause a method to be performed" where "said method" comprises the method

outlined in claim 1. *Id.* at 9:53–10:10, 10:25–46.

A. "Each of said global nets within said second subset routed by one of said threads in isolation of said second subset's other global nets but in respect of the routes of said subset of global nets"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"Each of said global nets within said second subset routed by one of said threads in isolation of said second subset's other global nets but in respect of the routes of said subset of global nets"	Each global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset and where the routing is in respect of said [first] subset of global nets	Each global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset, and the resulting routing does not conflict with routings of the first subset of global nets	Each global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset, and the resulting routing does not conflict with routings of the first subset of global nets

The parties dispute whether the claim language should entirely prohibit any conflicts between routings of subsequent subsets. Siemens asserts that the patent prohibits any such conflicts. Dkt. No. 114 at 9–10. It relies on the specification's statement that "the nets within the second window [subset] are routed so as not to conflict with the routed nets from the first window [subset]."[3] '614 Patent at 5:8–9. The broader context of this statement is the following:

> "In an embodiment, each thread routes its respective net in isolation from the other nets within the net's window but not previously routed windows. For example, as a simple example, assume a first window of nets is concurrently routed. Then, the next—second—window of nets is selected from the ranked net list. The nets within the second window are routed so as not to conflict with the routed nets from the first window. However, in an embodiment, the nets within the second window are routed in isolation of one another. As such, no conflicts should exist between nets within the first window and nets within the second window. However, conflicts may exist between nets within the second window."

Id. at 5:2–14.

Synopsys argues that Siemens focuses too narrowly on one embodiment of the patent, Figure 5, which "provides a simple example that demonstrates how conflicts may be detected and

[3] The parties agree that a "subset" is also referred to as a "window." *See* Dkt. No. 113 at 9; Dkt. No. 126 at 9.

resolved." '614 Patent at 5:35–36. Figure 5 "simplistically assumes that multiple routes cannot exist within the same tile" and therefore all conflicts between routes are eliminated. *Id.* at 6:11–12, 22–23.

In contrast, Synopsys points to another embodiment in column 6 where the patent expressly states that "multiple nets within a same tile is permitted." *Id.* at 6:23–25. For these more complicated embodiments that involve routing more than one net through the same tile, the patent allows "permissible" conflicts between routes. '614 Patent at 6:33. "Each tile is modeled so as to contain a 'bucket' of track resources. Each time a net is routed through a tile a unit of track resources is subtracted from the bucket amount." *Id.* at 6:23–32; Dkt. No. 126 at 22. A "permissible" conflict is when the value of the bucket resource is not below zero (i.e., the tile has enough resources to entertain the route) because then the tile can handle the routing request. *Id.* at 6:34–38. In contrast, an "impermissible conflict" is when "the remaining track resources are below [zero] (i.e., the tile does not have enough resources to entertain the route." *Id.* at 6:38–41.

As Siemens contends, this section in column 6 does not refer to the routing between *different* subsets. Dkt. No. 114 at 10. This section distinguishes Figure 5, which concerns checking for conflicts between routes of nets within the *same* subset, and provides an embodiment where "permissible conflicts" may exist. Synopsys's expert, Dr. Carley, admitted that Figure 5 refers to conflicts within the same subset, not conflicts between different subsets:

> "Q: Does Figure 5 of the '614 Patent concern checking conflicts between routes of nets within the same subset?
>
> A: Since – yes. I mean, implicitly it does because we know there won't be conflicts created with prior routes because the algorithm was designed not to create -- an algorithm following the patent's teachings would be designed not to create conflicts with one -- routes from prior windows. So, the conflict detection referred to in Figure 5 would implicitly be talking about conflicts between routes that were all created within the current window."

Dkt. No. 114-5 ("Carley Depo.") at 16:12–21. As a result, the disclosures in column 6 that are related to Figure 5 are irrelevant because they concern only conflicts between routings of nets

within the same subset.[4] Dkt. No. 114 at 10.

Synopsys asserts that there is "no principled reason why 'permissible conflicts' would also be allowed between routes in the same subset, and not between routes of different subsets." Dkt. No. 118 at 7. The principled reason, however, is that the patent expressly allows for conflicts between routes in the same subset, '914 Patent at 6:22–41, but states that the routes between subsets should not conflict, *id.* at 5:8–13. Synopsys argues that these statements in column 5 are limited to a narrow embodiment. *Id.* at 10–11. But Synopsys's own expert opined that a skilled artisan would have interpreted this term in light of the patent's column 5 disclosures "not to conflict" with routings of the first subset of nets:

> "Q: Do the statements in Column 5, Lines 8 through 13 that we read, do those statements address the same issue that is being addressed in the last step of Claim 1; namely, that each net in the second subset is routed in respect of the routes of said subset of global nets? Is it speaking to the same issue?
>
> [Objection to form]
>
> A: Yes. This is – this is all about what information do the threads have available and how do they use that information in performing routing at various stages of the algorithm. And it is well explained in the specification, and I would say a POSITA would have understood the Column 5 language very clearly and would have interpreted the claim language in light of that."

Carley Depo. at 12:4–13:13. Siemens's construction is proper.

B. "ranking shorter length and lower fan-out nets over longer length and higher fan-out nets"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"ranking shorter length and lower fan-out nets over longer	Plain and ordinary meaning/no construction	Indefinite Alternatively: sorting a first pair of nets	Plain and ordinary meaning/no construction

[4] During the Claim Construction Hearing, the parties disagreed whether Synopsys mischaracterized Carley's testimony when it relied on pages 76–77 of Carley's deposition to argue that Carley stated that his report accurately reflected his opinion that permissible conflicts are allowed between routes of different subsets. Dkt. No. 126 at 25. I reviewed Carley's deposition and agree with Siemens. During his deposition, Carley confirms that his opinion in paragraph 49 remains the same but paragraph 49 quotes the patent's language on "permissible conflicts," which does not refer to conflicts with routes from the prior subset. *See* Carley Depo. at 76–77; Dkt. No. 113-3 ("Carley Rep.") ¶ 49.

length and higher fan-out nets”	necessary	ahead of a second pair of nets, wherein each of the first pair of nets has less spatial extent and fewer pins driven by the net than each of the second pair of nets	necessary

Synopsys argues that a skilled artisan would understand the words “ranking,” “shorter/longer,” and “higher/lower,” and therefore no construction is necessary. Dkt. No. 113 at 11. Siemens asserts two objections: (1) the term is indefinite; and (2) a plain meaning interpretation would not resolve the dispute. Dkt. No. 114 at 11.

1. “Length” and Ranking Criteria

First, Synopsys argues that a skilled artisan would understand that “length” in the routing context means an estimate because the common industry practice is to estimate net length and use estimation models. Dkt. No. 113 at 12; Dkt. No. 126 at 32. Siemens contends that the term is indefinite because a POSITA would not know whether he or she is infringing the patent if “length” is a predicted estimate. Dkt. No. 114 at 11. According to Siemens, the boundary is also unclear because different length-prediction techniques would produce different rankings and the patent does not articulate a method by which the nets are ranked. *Id.* For example, a skilled artisan could pick a non-length criterion for ranking nets in a particular order, but later identify a length-prediction method under which that order happens to rank nets from shortest to longest and therefore violate the patent. *Id.*

It is irrelevant which method a practitioner uses for ranking because the patent teaches ranking by length for any estimation method. Dkt. No. 118 at 8. Siemens’s reliance on *Dow Chemical Co. v. Nova Chemicals Corp. (Canada)*, 803 F.3d 620 (Fed. Cir. 2015), and *Teva Pharmaceuticals USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335 (Fed. Cir. 2015) is misplaced. Both cases required a calculation of an exact value (e.g., exact molecular weight or exact strain-hardening coefficient) to ascertain whether the practice infringed on the claim. *Dow*, 803 F.3d at 624–25; *Teva*, 789 F.3d at 1338. The Federal Circuit held that the terms were indefinite

United States District Court
Northern District of California

because there were multiple methods of measurement that could yield different results but the patents did not expressly discuss which to use. *Dow*, 803 F.3d at 634; *Teva*, 789 F.3d at 1343.

In this case, the '614 Patent merely covers a method by which to rank nets as a preliminary step before the actual routing of nets. Unlike *Dow* and *Teva*, the '614 Patent does not set forth a numerical range by which nets of certain lengths might fall within or out of the patent's scope. The purpose of calculating an estimated length is merely to obtain a basis for ranking, not to determine whether the practice oversteps the claim boundary. Only once a person reaches the ranking step would he or she need to worry about whether their ranking method infringes the patent, so the dispute over metrics raised by Siemens fails to reach the essence of the claims. As Synopsys argues, the patent merely states that once *any* lengths are determined, the ranking method under the patent requires ranking from shortest to longest. Dkt. No. 126 at 38. I agree with Synopsys that the term is sufficiently definite and that no construction is necessary.

2. "Length" and "Fan-Out" as Weighted Factors

Siemens further argues that ranking the nets based on two independent criteria, length and fan-out, is indefinite because the two metrics are not always correlated. Dkt. No. 114 at 12. Both Synopsys and Siemens agree that there will be situations in which either (1) the first net is longer and has fewer pins than the second net, i.e., a lower fan-out, or (2) the first net is shorter and has more pins than the second net, i.e., a longer fan-out. Dkt. No. 113 at 12; Dkt. No. 114 at 12. In addressing this conundrum, Synopsys argues that the specification provides for calculating a factor that is equal to either the weighted sum or the product of the net's length and fan-out, allowing for ranking by this created metric. Dkt. No. 113 at 12. Siemens responds that the calculated factor is not present in Synopsys's proposed definition, which would prevent a POSITA from knowing the boundary of the patent. Dkt. No. 114 at 12.

As Synopsys asserts, however, a POSITA would understand how to scale length and fan-out to take both into account from the specification. In determining the plain and ordinary meaning, courts look to "[t]he written description and other parts of the specification" for "contextual light[.]" *Aventis Pharm. Inc. v. Amino Chemicals Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013). Similarly, "in assessing definiteness, claims are to be read in light of the patent's

specification." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 908 (2014). In this case, the specification states,

> "According to the specific embodiment of FIG. 2, the remaining nets are further sorted such that shorter and lower fan-out nets are routed before longer and higher fan-out nets (on the theory that shorter and lower fan-out nets are more difficult to re-route if involved in a conflict). Here, to accomplish this sorting, *a factor is calculated that weighs both a net's length and fan-out*. For example, a first number is used to gauge a net's length and a second number is used to gauge the net's fan-out. The product or summation of the two numbers determines the net's factor. The nets can then be sorted based on the factor."

'614 Patent at 3:38–43 (emphasis added). This resolves the conundrum of ranking under this claim element where the nets are long but the fan-outs are short and vice versa because one can rank by the sum or product of the values.

Siemens also requests that I clarify whether both the fan-out and length values must be used under this claim term. Dkt. No. 126 at 35–36. It asserts that Carley "essentially said and/or," meaning both values were not necessary under the claim term. *Id.* at 36; *see* Carley Depo. at 41–42. To the contrary, although Carley testified that the claim element could encompass ranking that considers one value but not the other, Carley did not state that only one value should be used. *Id.* Instead, he explained that under the multiplication method, for example, if the fan-out was set to one then the product would only be the value of the length. *Id.* at 41. Similarly, under the weighted sum method, if the value for the length is zero, then the sum would be the value of the fan-out. *Id.* at 42. Synopsys did not address this point directly, but based on Carley's testimony, both the fan-out and length values are used, even in scenarios where one value would not change the value of the sum or the product. As a result, both the fan-out and length values must be used under this claim term.

Siemens argues that a jury would not be able to understand the plain meaning of this term because even Synopsys's expert, Carley, was confused by the term's meaning. Dkt. No. 126 at 31–32 (citing Carley Depo. at 37–42, 72–75). When asked whether the claim term can encompass ranking by "timing slack" in a hypothetical, Carley first responded that it did but then conceded that it did not after Siemens pointed out that the specification indicates that ranking by "timing

slack" is a "different" ranking scheme than the term at issue. Dkt. No. 114 at 12–13. Synopsys asserts that Carley's understanding of the term in the abstract hypothetical is irrelevant because "in assessing definiteness, claims are to be read in light of the patent's specification." *Nautilus*, 572 U.S. at 908. I agree. Notwithstanding Carley's testimony, Siemens's argument that the specification indicates that the term does not encompass ranking by "timing slack" shows that a POSITA would understand the scope of the term based on the specification and therefore construing the term as its plain and ordinary meaning is proper.

III. '655 PATENT

The '655 Patent is titled, "Fixing Design Requirement Violations in Multiple Multi-Corner Multi-Mode Scenarios." Dkt. No. 1-1, Ex. 6 ("'655 Patent"). A chip design must satisfy pre-manufacture criteria to ensure proper functioning upon physical implementation. '655 Patent at 1:19–21. If a violation is detected, incremental adjustments known as Engineering Change Orders ("ECOs") are required. *Id.* at 3:38–40. The chip design needs to be vetted for violations across combinations of process and operating conditions. *Id.* at 1:31–33. The '655 Patent developed a multi-scenario ECO database, which stores parameters and allows for a quick estimation of an ECO's impact across multiple scenarios. *Id.* at 4:61–67.

Claim 1 recites,

> "A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:
> receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;
> receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO data base stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and
> determining, by using one or more processors, an ECO to fix one or more design requirement violations, wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database."

Id. at 9:54–67. Independent claim 11 is similar but relates to "[a] non-transitory computer-readable storage medium storing instructions that, when executed by a computer, cause the computer to perform a method for fixing design requirement violations in a circuit design in multiple scenarios." *Id.* at 10:25–42. Independent claim 21 recites,

> "A system, comprising:
> a processor; and
> a memory, storing:
> a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;
> a multi-scenario engineering change order (ECO) data base, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and
> instructions that, when executed by the processor, cause the system to determine an ECO to fix one or more design requirement violations, wherein said deter mining includes estimating parameter values for circuit objects in at least some of the multiple scenarios using parameter values stored in the scenario image and the multi-scenario ECO database."

Id. at 11:4–20.

A. "A multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"A multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios"	A database separate from the scenario image that stores a subset of parameter values for a subset of circuit objects in the multiple scenarios	A database separate from the scenario image that stores a subset of parameter values for a subset of circuit objects in the multiple scenarios, which is only a small fraction of the information stored in the scenario image	A database separate from the scenario image that stores a subset of parameter values for a subset of circuit objects in the multiple scenarios

The parties dispute whether a defining characteristic of the multi-scenario ECO database is that the database is always a small fraction of the information stored in the scenario image. Siemens argues that its proposed definition is consistent with the patent's use of the word "subset." Dkt. No. 114 at 14–15. It asserts that the database's ability to store a "subset of the parameter values for only a subset of the circuit objects" comports with the conclusion that the database must contain only a fraction of the information stored in the scenario image. *Id.* Although the '655 Patent explains that "[t]he information stored in a multi-scenario ECO database *can* be a small fraction of the information stored in a scenario image," Synopsys asserts that the nature of the database is not limited to this definition. '655 Patent at 6:5–7 (emphasis added); Dkt.

No. 113 at 15. As Synopsys's expert, Dr. Stephen Edwards, explains, such a configuration is "only an example, not a requirement." Dkt. No. 113-5 ("Edwards Rep.") ¶ 33; *see also* *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1310 (Fed. Cir. 2017) ("[W]hile we read claims in view of the specification, of which they are a part, we do not read limitations from the embodiments in the specification into the claims.").

Synopsys contends that an entire set can be a subset of itself; that the database can be substantially smaller does not mean that it must be smaller. Dkt. No. 118 at 9–10 (citing JCCS, Ex. 4 at 6–7). As an example, Synopsys provides the situation where the system involves a small circuit but needs to assess the impact of a relatively large ECO. Dkt. No. 126 at 44. In that case, the database may want to account for all the circuit objects in assessing the modification, rather than storing only a portion of the values needed to check across multiple scenarios. *Id.*

Synopsys also asserts that there are multiple ways to store the database alongside a scenario image in memory, including reducing the size of the scenario image without making the database information "only a small fraction" of the scenario image. Dkt. No. 113 at 15; *see* Edwards Rep. ¶ 33 ("If the scenario image is made smaller, the denominator of the fraction representing the ratio between the scenario image size to the multi-scenario ECO database size gets larger."). Siemens counters that Synopsys cannot escape the limitation by presenting alternate database configurations that are not explicitly disclosed in the patent. Dkt. No. 114 at 14. But Edwards testified that the practice of compressing the scenario image for the benefit of fitting it alongside the database in memory would be standard practice for a POSITA at the time. Dkt. No. 114-6 ("Edwards Depo.") at 49:17–50:12. Accordingly, I agree with Synopsys's proposed construction in which the database's fractional quality is permitted, but not required.

B. "determine[e/ing . . .] an ECO to fix one or more design requirement violations"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"determin[e/ing . . .] an ECO to fix one or more design requirement violations, wherein	Plain and ordinary meaning/no construction necessary	Indefinite	determin[e/ing . . .] an ECO to fix one or more design requirement violations, wherein

said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database”	Alternatively: Construe the “wherein” limitation as “identifying an ECO to fix a design requirement violation in the scenario and checking that ECO against at least some of the multiple scenarios by estimating parameter values based on parameter values stored in the scenario image and the multi-scenario ECO database”		said determining includes identifying an ECO to fix a design requirement violation in the scenario and checking that ECO against at least some of the multiple scenarios by estimating parameter values based on parameter values stored in the scenario image and the multi-scenario ECO database

The parties dispute whether a POSITA would understand the scope of the term with reasonable certainty. The process by which an ECO is checked across multiple scenarios using the multi-scenario ECO database involves multiple decision points. First, a scenario image is loaded from storage. *Id.* at 4:21–22. If there is a design requirement violation, an ECO is determined for this first scenario. *Id.* at 4:24–26. Subsequent scenarios are loaded, one at a time, to check whether the ECO from the first scenario will create new design requirement violations or exacerbate existing violations in the subsequent designs. *Id.* at 4:29–33. In some cases, estimated parameter values, based on the information contained in the first scenario, may be required to determine whether the ECO will create or worsen new design requirement violations in the second scenario. *Id.* at 6:58–65. If no new or worse violation is found in a subsequent scenario, the system may keep loading scenario images, one at a time, to check whether the ECO from the first scenario will work. *Id.* at 4:35–39. On the other hand, if there is a new or worse violation detected, the system may reject the ECO from the first scenario and start over by determining a new set of ECOs to apply to the first scenario. *Id.* at 4:33–35.

Siemens asserts that the term is indefinite because it is unclear which of the following distinct steps—the “determining,” “estimating,” or “checking” step—apply under this term. Dkt. No. 114 at 15–16. It argues that the claim language is internally inconsistent because the term

states that the "determining" step includes "estimating" when the specification distinguishes the two. Dkt. No. 114 at 18; Dkt. No. 126 at 49–50. As a result, a POSITA would not know whether the "determining" term encompasses "estimating" and/or "checking." Dkt. No. 114 at 17.

I disagree. There is no internal inconsistency because "the claim language includes a 'wherein' clause that unambiguously limits the claimed determining steps to those that include estimating parameter values." Dkt. No. 118 at 10. Synopsys's expert opines that "a POSITA would understand with reasonable certainty that in the context of the '655 Patent the determining term requires both identifying a possible fix (based on the scenario image) and checking whether the possible fix is suitable (based on parameter values stored in the scenario image and the multi-scenario ECO database" in at least some scenarios). Edwards Rep. ¶ 44. Because the claim language indicates that estimation is a part of "determining," "determining" can also encompass "checking" because parameter estimation is a way to check the ECO. [5] *Id.* ¶¶ 43–44.

The claim, however, does not require checking an ECO in all scenarios because the claim makes clear that "estimating parameter values for circuit objects" need only occur "in at least some of the multiple scenarios."[6] *See* '655 Patent at 9:65–66; Edwards Rep. ¶ 46; Dkt. No. 126 at 55. Likewise, the abstract explains that "the system can determine an [ECO] to fix one or more design requirement violations, which *can involve* estimating parameter values." '655 Patent Abstract (emphasis added). For example, if there were no design requirement violation detected in the first scenario image, no ECO would be determined, and hence there would be no need for the

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[5] Siemens also argues that the current patent language is confusing because it is unclear whether there is a requirement to apply the ECO to a circuit. Dkt. No. 114 at 17–18. According to Siemens, an artisan may interpret "determining . . . an ECO to fix" as applying the final ECO to fix the design. *Id.* But as both parties acknowledge, the claim element does not recite applying an ECO to a circuit in order to fix the violation. *Id.*; Dkt. No. 118 at 11; *see also* '655 Patent at 5:34–37 (stating that the application "may either commit the determined ECOs to the circuit design or store the ECOs in storage so that the ECOs can be committed to the circuit design later."). Siemens also does not point to any claim language that suggests that the patent requires applying the final ECO. There is no confusion about the scope of the term in this regard.

[6] Contrary to Siemens's argument, Edwards's testimony that the claim language does not explicitly require "checking" is therefore consistent with his testimony that "determining" can encompass "checking" the ECO for violations in some scenarios. *See* Dkt. No. 114 at 17 (citing Edwards Depo. at 21–22).

subsequent estimating and checking across multiple scenarios. *See* Dkt. No. 126 at 55.

Furthermore, the purpose of the '655 Patent is to replace the archaic method of "loading additional scenarios one-by-one to check whether the ECOs are suitable." Edwards Rep. ¶ 44. Synopsys's expert explains how the conventional method of loading single scenario images involved determining, estimating, and checking. *Id.* A POSITA would understand that the novelty of the multi-scenario ECO database behind the patent specifically serves to streamline these steps in the interest of optimizing chip development. *See id;* Dkt. No. 48 ("This method improves upon the prior art . . . thereby improving the likelihood that an ECO will work across multiple scenarios and reducing the need to backtrack or redo ECOs further along in the process"). Unless "determining" includes estimating and checking, the basis of the patent's novelty would be lost. I will therefore construe the "wherein" clause in accordance with Synopsys's alternative construction: "identifying an ECO to fix a design requirement violation in the scenario and checking that ECO against at least some of the multiple scenarios by estimating parameter values based on parameter values stored in the scenario image and the multi-scenario ECO database." Dkt. No. 118 at 12.

C. "scenario image"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"scenario image"	Information required to detect and/or fix design requirement violations in a circuit design in a particular scenario	Information from a non-volatile storage device, required to detect and/or fix design requirement violations in a circuit Alternatively: Information from a storage location that is not computer memory, required to detect and/or fix design requirement violations in a circuit	Information required to detect and/or fix design requirement violations in a circuit design in a particular scenario

Synopsys and Siemens dispute whether the claim mandates the use of non-volatile storage

for the scenario image received by the system. Siemens argues that the limitation is necessary because the patent's only examples of scenario images involve the use of disks or other non-volatile storage. Dkt. No. 114 at 19. Alternatively, Siemens proposes a limitation that precludes at minimum the storage of the scenario image in computer memory. Dkt. No. 126 at 57. It argues that a skilled artisan "would understand the patent to describe receiving in memory a scenario image from a non-volatile storage area, such as storage 308 depicted in Fig. 4 as distinct from volatile memory 406 in Fig. 4." Dkt. No. 102 ¶ 107; *see also* Dkt. No. 114 at 19.

Synopsys responds that the claim may include, but is not limited to, the use of non-volatile storage. Dkt. No. 113 at 18. For example, the specification recites,

> "The data structures [such as a scenario image] and code described in this disclosure can be partially or fully stored on a computer-readable storage medium . . . [a] computer-readable storage medium includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media, now known or later developed, that are capable of storing code and/or data."

'655 Patent at 9:19–27. It argues that Siemens's construction improperly limits the proposed definition to characteristics of a specific embodiment illustrated in the patent. *Id.* "Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004). In this case, there is no clear intention to limit the claim scope as evidenced by the specification permitting the use of volatile storage. *See* '655 Patent at 9:22–27; *see also id.* at 9:15–19 ("[T]he present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.").

Siemens asserts that its proposed construction captures the "essential heart of the claims" as argued by Synopsys during the prior briefing on the 35 U.S.C. § 101 dispute, namely that each "scenario image" is received from non-volatile storage one at a time. Dkt. No. 126 at 57. Synopsys argued that under the '655 Patent, "the amount of time required to check the impact of

an ECO on other scenarios is substantially reduced because swapping scenario images in and out of memory (i.e., to and from disk) is no longer required." *Id.* In my prior order addressing the Section 101 argument, I also acknowledged that the '655 Patent "claims a method that improves the 'efficient functioning of computers' by identifying a way to check ECOs across multiple scenarios at a time – despite computer memory limitations – and reducing the need to engage in the time-consuming process of loading different scenario images from the computer's storage to memory." Dkt. No. 48 at 17; *see* Dkt. No. 126 at 56–57.

Synopsys responds that Siemens misconstrues the driving concept behind the improved efficiency of the '655 Patent by narrowly focusing on the patent's replacement for the method of "swapping each of the corresponding scenario images to and from disk," a type of non-volatile storage. Dkt. No. 118 at 12. It indicates that the description of storage in the '655 Patent also pertains to the origin of the initial scenario image that would be loaded into the system and used to determine the impact across the rest of the scenario images residing in memory. *See* Dkt. No. 118 at 12 ("That does not change whether the *first* scenario image originates from volatile or non-volatile memory") (emphasis added). Siemens counters that this is "irrelevant because loading the scenario image into memory does not preclude it being received from a non-volatile storage device." Dkt. No. 114 at 19.

As Synopsys points out, however, there is no requirement that precludes an initial scenario image being received from a volatile storage device. Dkt. No. 126 at 58. It distinguishes the patent's uniqueness by its innovation upon the iterative loading of subsequent scenario images, emphasizing that the choice of storage medium for the initial scenario image remains within the discretion of the designer. *Id.* at 59. Siemens's proposed construction based on one example of storage shown in the patent is improperly exclusive of available storage options. I agree with Synopsys that the proposed construction should not limit the claim solely to non-volatile storage of the scenario image.

IV. '915 PATENT

The '915 Patent is titled "Interconnect-Driven Physical Synthesis Using Persistent Virtual Routing." Dkt. No. 1-1, Ex. 4 ("'915 Patent"). Physical synthesis is part of the design flow for

designing computer chips; "accurately predicting interconnect delays has become one of the critical steps in high performance integrated circuit (IC) designs." '915 Patent at 1:12–14. Differences in estimated pin-to-pin delays and parasitics during circuit optimization at the pre-route stage from actual delays and parasitics after routing can lead to wasted effort during the pre-routing stage, thereby requiring expensive post-route optimization. *Id.* at 1:12–15, 1:21–31, 6:35–43. The inventors of the '915 Patent recognized that if one could guarantee correlation of the parasitics and delays for the most sensitive nets between pre-routing optimization and post-routing, it would minimize the routability impact. *Id.* at 3:17–24, 6:43–67. They also recognized that if these types of nets could be routed at an earlier point than normal routing, then their routes can be used to make optimization decisions. *Id.* at 6:65–7:8.

Claim 1 recites,

> "A method of performing physical synthesis using persistence-driven optimization, the method comprising:
> using a processor,
> ranking nets in a design based on unpredictability and expected quality-of-result impact;
> selecting a first predetermined top percentage of the ranked nets as first persistent nets;
> performing timing-driven global routing on the first persistent nets;
> back-annotating a timing graph with actual delays and parasitics determined by performing the timing-driven global routing on the first persistent nets;
> running synthesis for the nets in the design using the actual delays and the parasitics for the first persistent nets, wherein the synthesis maintains and updates routing for the first persistent nets;
> re-ranking the nets in the design after synthesis based on unpredictability and expected quality-of-result impact;
> selecting a second predetermined top percentage of the re-ranked nets as second persistent nets;
> performing timing-driven global routing on the second persistent nets that had not been selected among the first persistent nets;
> performing global routing on the nets of the design while maintaining existing routes of the second persistent nets; and
> outputting a final layout of the design based on the global routing."

Id. at 16:55–17:16. Independent claim 35 is similar but refers to "[a] computer readable storage device comprising computer instructions that, when run on a computer, generate signals to control the process steps" outlined above. *Id.* at 19:6–32. Independent claim 51 recites,

> "A persistence-driven optimization tool executable by a computer and stored on a computer-readable storage device, the persistence-driven optimization tool comprising:

> a net selection module for filtering and ranking nets in a design based on unpredictability and expected quality of-result impact, the net selection module outputting a list of selected nets;
> an interconnect-synthesis module for performing timing driven topology generation, layer assignment, and global routing of the selected nets, the interconnect-synthesis module outputting persistent global routes having actual parasitics and delays for the selected nets;
> an interconnect-aware circuit optimization module for driving placement-driven optimization based on the actual parasitics and delays for the persistent global routes while maintaining and updating these persistent routes, the interconnect-aware circuit optimization module outputting an optimized design with the persistent global routes; and
> a global route translation and preservation module for translating the persistent global routes into a format recognized by the routing database as pre-existing global routes to be preserved during global routing, the global route translation and preservation module outputting a design file suitable for global routing followed by subsequent routing steps such as track assignment and detailed routing and post-route optimization."

Id. at 20:39–64.

A. "maintains and updates routing," "maintaining [the] existing routes," "maintaining and updating . . . persistent routes," "persistent nets," and "persistent global routes"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"maintains and updates routing" & "maintaining [the] existing routes" & "maintaining and updating . . . persistent routes" "persistent nets" "persistent global routes"	<u>maintains and updates routing / maintaining and updating . . . persistent routes:</u> updat[es/ing] the routes incrementally as needed to maintain the validity of the route as much as possible <u>maintaining [the] existing routes:</u> maintaining the validity of the existing routes as much as possible <u>persistent nets:</u> nets whose global routes are guaranteed to be preserved as much as	<u>maintains and updates routing / maintaining and updating . . . persistent routes:</u> Modifies/Modifying without modifying the persistent (unchanged) routes <u>maintaining [the] existing routes:</u> leaving routes of persistent nets unchanged <u>persistent nets:</u> nets whose global routes are guaranteed to be preserved through subsequent stages	<u>maintains and updates routing / maintaining and updating . . . persistent routes:</u> updat[es/ing] the routes incrementally as needed to maintain the validity of the route as much as possible <u>maintaining [the] existing routes:</u> leaving routes of persistent nets unchanged <u>persistent nets:</u> nets whose global routes are guaranteed to be preserved as much as

	possible through subsequent stages <u>persistent global routes:</u> global routes that are guaranteed to be preserved as much as possible through subsequent stages	<u>persistent global routes:</u> global routes that are guaranteed to be preserved through subsequent stages With or without these proposed constructions: Indefinite.	possible through subsequent stages <u>persistent global routes:</u> global routes that are guaranteed to be preserved as much as possible through subsequent stages

The inventors of the patent sought to resolve the problem of delay mispredictions between pre-route delay estimates and post-route estimates by routing certain nets that have greater impact on circuit performance at an earlier point than normal routing. Dkt. No. 119. The parties dispute two issues: (1) whether the terms are indefinite as to which route changes, if any, are permitted; and (2) whether "maintaining [the] existing routes" of second persistent nets permit any changes.

1. Indefiniteness

Siemens asserts that the following claim terms contradict portions of the specification and are indefinite: "maintains and updates routing," "maintaining and updating . . . persistent routes," "persistent nets," and "persistent global routes." Dkt. No. 114 at 20. Because these terms are coined terms that were not known to artisans at the time of the patent's filing, the "duty thus falls on the patent applicant to provide a precise definition for the disputed term." *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F. 3d 1295, 1300 (Fed. Cir. 2004). Siemens argues that rather than providing a precise definition, the specification and claims are internally inconsistent. Dkt. No. 114 at 20.

The patent defines "persistence" as "guaranteeing the routes for some judiciously selected nets before routing (e.g. during placement-based optimization) and then using actual parasitics and net delays for those selected nets during subsequent placement-based optimization steps." '915 Patent at 3:27–31. Synopsys's expert, Dr. David Pan, testified that the "actual parasitics and net delay" in the patent's definition of "persistence" are "as accurate as one can get" after the global routing stage. Dkt. 113-9, Ex. 8 ("Pan Depo.") at 31:24–33:17. Portions of the patent define "persistent nets" as "nets whose global routes set during placement are 'guaranteed' to be

'preserved' and 'maintained' through the subsequent circuit optimization and routing stages." *Id.* (citing '915 Patent, 3:27–33, 5:7–12, 5:64–6:5, 7:9–15). In contrast, other portions of the patent allow for "updat[ing] routing for the first persistent nets," "incrementally patching" the global routes to minimize the impact of pin changes on the global route, and "maintain[ing] the validity of the persistent global routes as much as possible." '915 Patent at 7:22–27, 8:13–17, 11:5–25, 17:3–4.

Contrary to Siemens's argument, these parts of the specification are not inconsistent with the rest of the patent; they simply address how to resolve problems that arise in a specific scenario, i.e., during certain optimization techniques. The patent does not teach that the persistent nets cannot be modified. Dkt. No. 118 at 13. Instead, it recognizes that "'optimization can indeed cause small perturbations to the pin locations as a result of cell sizing, buffer insertion, or other transforms,' and explains that the inventive interconnect-driven physical synthesis technique using persistent virtual routing 'has the capability to handle many of these changes through the patching of the persistent global routes.'" Pan Rep. ¶ 28 (citing '915 Patent at 7:22-27, 8:13-17).

According to Pan, "[p]atching refers to applying small corrections to account for the small perturbations to maintain the general global route." *Id.* Another part of the specification also "explains how the deviations from the persistent global routes caused by common optimization can be handled." *Id.* ¶ 29.

> "Note that commonly used optimization techniques, such as cell sizing and buffer insertion, can cause changes to the pin locations and even interconnect topologies, thereby potentially rendering the persistent routings invalid. Therefore, interconnect-aware circuit optimization module 503 can implement several algorithms to treat persistent nets preferentially so that cell sizing and buffer insertion maintains the validity of the persistent global routes as much as possible. This preferential treatment can include incrementally patching the global routs at the pin locations subsequent to cell sizing as well as global route inheritance from persistent nets that are split into multiple nets after buffer insertion. More precisely, the routes for the net nets obtained after one or more buffers have been inserted into a persistent net can be derived from the route for the original net. In one embodiment, the pre-routing stage buffer insertion algorithms can be modified to make them aware of the global routes for persistent nets while deciding the topological and geometric location of a new buffer. This modification allows the recovery of a substantial portion of the persistent routing for the newly formed nets from the routes of the original persistent nets (and thus, the use of accurate parasitics for

these new nets).”

’915 Patent at 11:4–25. Pan explains that “the routes of persistent nets are to be maintained when possible, and where an optimization causes a deviation, the routes are to be updated or nets patched to maintain as much as possible of the route.” Pan Rep. ¶ 28.

Siemens responds that if a POSITA chose to make changes, he or she would not know which changes would fall outside the claim elements’ boundary because the patent does not define the phrase “as much as possible.” Dkt. No. 114 at 22. It points out that Synopsys asserts that the global route “remains essentially the same, except for the minor deviations,” Dkt. No. 113 at 20, but it does not cite to any objective criteria for assessing when a route is not “essentially the same,” or a deviation is not “minor.” *Id.*

Siemens relies on *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1363 (Fed. Cir. 2018) to argue that Synopsys’s construction lacks objective boundaries, but the case is distinguishable. In *Berkheimer*, the Federal Circuit held that a claim term, “minimal redundancy,” was indefinite because the specification used inconsistent terminology to describe the level of redundancy that the invention achieved, i.e., “minimiz[ing] redundant objects,” “eliminating redundancy,” and “reducing redundancies.” *Berkheimer*, 881 F. 3d at 1363–64. The only example in the specification exhibited no redundancy but the claim language did not require the elimination of all redundancies, and therefore the specification “contain[ed] no point of comparison for skilled artisans to determine an objective boundary of ‘minimal’ when the [invention] includes *some* redundancies.” *Id.* at 1364 (emphasis in original). The patentee’s expert also did not respond to the defendant’s expert’s testimony that the patent failed to inform a skilled artisan of the claim term with reasonable certainty. *Id.*

In contrast, the claim term “maintaining and updating . . . persistent routes” is not internally inconsistent because the patent explains when the routes are updated to maintain the routes, i.e., during certain optimization techniques. Further, although the Federal Circuit has held that a single example in a lengthy written description cannot provide objective boundaries for a facially subjective claim term, it recognizes “that a patent which defines a claim phrase through examples may satisfy the definiteness requirement.” *Interval Licensing LLC v. AOL*, Inc., 766

F.3d 1364, 1373 (Fed. Cir. 2014); *see e.g.*, *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1332 (Fed. Cir. 2010) (holding that the term "not interfering substantially" was sufficiently definite because a skilled artisan could use "the examples in the specification to determine whether interference with hybridization is substantial"). In this case, a skilled artisan would understand which deviations allow for incremental patching because the patent provides the following examples.[7] For cell sizing optimizations, the patent indicates that "the global route can be patched at the pin locations subsequent to cell sizing to maintain the global route before and after the cell." Pan Rep. ¶ 30. For buffer insertions, "the new nets on each side of the inserted buffer can be derived from the global route of the original net such that the global routes of the new nets follow the global route of the original net before and after the inserted buffer." *Id.*; *see also* Pan Depo. at 47–48 (inserting a buffer would change the delay of the global route but not the parasitics); Robins Depo. at 218–19 (inserting a buffer would not "really chang[e] the routing of the wire").

Siemens argues that if these changes are made then the estimated parasitics and delays will change from the original global route and will no longer be "actual" or an "accurate" value, as Pan testified. *Id.*; Dkt. No. 126 at 62. It contends that a POSITA would not be able to reconcile these conflicting clues with reasonable certainty because he or she would not know whether to make any changes in order to avoid infringing the claims. Dkt. No. 114 at 22. Pan does not reconcile the "as much as possible" specification language with the "actual" values claim language. Dkt. No. 126 at 67–68. But as Synopsys contends, the claim language only says that the synthesis uses actual delays and parasitics; it does not say that it must keep them or that it cannot change them. Dkt. No. 126 at 65. The terms in Synopsys's construction are sufficiently definite.

2. "maintaining [the] existing routes"

Siemens argues that the claim language in claims 1 and 35, "maintaining the existing routes of the second persistent nets," means leaving the routes of the second persistent nets

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[7] Synopsys further clarifies that the '915 Patent "teaches incrementally patching a route *in response to deviations from common optimization techniques*, so as to maintain the route as much as possible." Dkt. No. 118 at 13–14 (emphasis in original). Therefore, Siemens's argument—that it would be possible to preserve the global route by forgoing the optional optimization—is irrelevant as the '915 Patent does not discuss "optional" or "required" optimizations. *Id.*; *see* Dkt. No. 114 at 21.

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unchanged. Dkt. No. 114 at 23. Pan testified that the second persistent nets are not updated, meaning they remain unchanged. Pan Depo. at 64:20–65:14, 67:20–68:16, 70:9–71:25 ("Q: So this describes that the second persistent nets are preserved without updating - - A: Correct, maintaining . . . Q: And maintaining means preserving without changing, correct? [Objection] A: Right. The word here used is maintaining."). Synopsys concedes that the second persistent nets remain unchanged. Dkt. No. 126 at 66. Siemens's construction of the "maintaining [the] existing routes" for the second persistent nets is correct. For the other terms, I adopt Synopsys's constructions.

B. "ranking [the] nets in a design based on unpredictability and expected quality-of-result impact" and "unpredictability and expected quality-of-result impact"

Term	Synopsys's Proposal	Siemens's Proposal	Court's Ruling
"ranking [the] nets in a design based on unpredictability and expected quality-of-result impact" "unpredictability and expected quality-of-result impact"	<u>ranking [the] nets in a design based on unpredictability and expected quality-of-result impact:</u> Plain and ordinary meaning/no construction necessary. *See* proposed constructions for "unpredictability . . . impact" and "expected quality-of-result impact." <u>unpredictability . . . impact:</u> condition where delay misprediction for a net can have a significant impact <u>expected quality-of-result impact:</u> likely timing/electrical criticality	<u>ranking [the] nets in a design based on unpredictability and expected quality-of-result impact:</u> sorting the nets based on a product of a function dependent on fanout, and a function dependent on slack, sensitivity, delay or half perimeter of the net's bounding box With or without this construction: Indefinite. <u>unpredictability and expected quality-of-result impact:</u> a function dependent on fanout and a function dependent on slack, electrical sensitivity, pin-to-pin delay, or half perimeter of the net's bounding box	<u>ranking [the] nets in a design based on unpredictability and expected quality-of-result impact:</u> Plain and ordinary meaning/no construction necessary. <u>unpredictability . . . impact:</u> condition where delay misprediction for a net can have a significant impact <u>expected quality-of-result impact:</u> likely timing/electrical criticality

		With or without this construction: Indefinite.	

The claims at issue recite ranking nets based on "unpredictability" and "expected quality-of-result impact." *See, e.g.*, '915 Patent at 16:58–59. Siemens argues that the terms are indefinite because (1) an artisan could not know with reasonable certainty when a particular ranking avoids this claim element; and (2) Synopsys's construction does not provide objective boundaries. Dkt. No. 114 at 24.

Synopsys asserts that its constructions are based on the intrinsic evidence and are sufficiently definite. Dkt. No. 113 at 23. Its construction for "unpredictability . . . impact" is "condition where delay misprediction for a net can have a significant impact." *Id.* at 24. The '915 Patent explains that the "difference in pin-to-pin delays and parasitics may significantly mislead the circuit optimization trajectory" between the pre-routing stage and post-route optimization and as a result "design convergence becomes difficult due to this unpredictability in the design flow." '915 Patent at 1:12–33. The patent further explains that the "unpredictability condition can be met by any net whose delay mis-prediction can have a significant impact (e.g. over 10% difference in the delay of the most critical path passing through that net)." *Id.* at 7:39–43. The patent also expressly defines "quality-of-result impact" ("QoR impact") as "likely timing/electrical criticality impact," which is consistent with the term as it would be understood generally by a POSITA in the context of the claimed invention. *See id.* at 7:32–35; Pan Rep. ¶ 55. In other words, the patent teaches "ranking based on criteria associated with unpredictability and expected quality of result-impact (e.g., fanout, sensitivity, etc.) and making a selection of those nets persistent, thereby preventing those nets from having a significant delay misprediction." Dkt. No. 118 at 15 (citing '915 Patent at 4:9–13, 13:20–32, 14:8–16, 16:59–17:4); Pan Rep. ¶¶ 14–15.

Siemens contends that a skilled artisan who seeks to avoid the claim element "has no objective measure by which to confidently confirm that her ranking of nets will not be deemed to be based on 'unpredictability.'" Dkt. No. 114 at 25. It argues that Synopsys's construction does not provide objective criteria for how to assess the "impact" of "delay misprediction," or what

degree of "impact" would qualify as "significant," or the bounds of "likely" timing/electrical criticality. Dkt. No. 114 at 25. This issue is irrelevant, however, because "the claims only require a *relative ranking* of nets 'based on unpredictability and expected quality-of-result impact.'" Dkt. No. 118 at 15 (emphasis in original).

Siemens recognizes that the patent explains that one measure of unpredictability is fan-out but it argues that the patent does not provide an "objective measure for *reliably* comparing the relative delay unpredictability of different nets" or "even a rule of thumb for comparing nets with the same fan-out." Dkt. No. 114 at 24 (emphasis in original); *see* '915 Patent at 13:20–21 (stating that "increasing the number of sink pins of a net (i.e., increasing its fanout) can result in greater unpredictability"). According to Siemens, a skilled artisan would not accept an interpretation that the claim element requires fan-out with reasonable certainty because the element does not explicitly say "fan-out," no one asserts that fan-out is the only property that can result in greater unpredictability, and it is unclear how to rank nets with the same fan-out. Robins Rep. ¶¶ 132–34.

It also contends that combining "unpredictability" with "expected quality of result impact" results in confusion because it is unclear how to balance the criteria. Dkt. No. 114 at 25. Siemens's expert acknowledges that the patent recites that, "this cost function can be a product of a function that depends on the electrical sensitivity of the net, a function that depends on the fan-out of the net, a function that depends on the delay of the net, and a function that depends on the slack of the net." Robins Rep. ¶ 145 (citing '915 Patent at 3:56–60). But he argues that "this kind of suggestion that the cost function can generally be the product of four other functions . . . does not narrow enough the potentially enormous number of mathematical combinations that the patent expects a skilled artisan to experiment with." *Id.* ¶ 146. As a result, Siemens contends that a skilled artisan would not have reasonable certainty concerning what ranking criteria would fall within the claim limitation. *Id.* ¶ 147.

But as Synopsys asserts, the patent's lack of disclosure of how to rank nets with the same fan-out or how to perform compound ranking does not render the terms indefinite because these are design choices that a POSITA can make. *Id.* Even if Siemens is correct that a skilled artisan would have an "enormous number of mathematical combinations to experiment with," the Federal

Circuit has held that "breadth is not indefiniteness." *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017).

Synopsys also contends that Siemens's construction is improper because it would exclude an embodiment illustrated in Figure 7 where only one cost function, based on sensitivity, is used for net ranking. *Id.* at 13:48–51 ("In one embodiment, steps 701/702, 703/704, 705/706, and 707/708 can be performed independently of one another, i.e. only one cost function is used for net ranking"); *Id.*, Fig. 7 (step 702: "Rank nets based on sensitivity"). "A claim construction that excludes a preferred embodiment [] is rarely, if ever, correct." *SanDisk Corp*, 415 F.3d at 1285 (internal quotation marks omitted). "Although the patent teaches that the unpredictability impact of two nets can be compared by using a cost function dependent on fanout (915 Patent at 13:20–24) and expected quality-of-results impact can be based on sensitivity, bounding box size, delay, and slack ('915 Patent at 4:9–13, 12:65–13:2, 13:28–32, 14:8–29), the patent does not teach that only those functions can be used." Dkt. No. 113 at 24.

Siemens argues that its construction encompasses the embodiment of Figure 7 because Figure 7 does not allow for ranking based on only one cost function; it allows for ranking based on fan-out and another condition. Dkt. No. 114 at 25. I disagree. The patent recites that Figure 7 "illustrates an exemplary ranking stage [] that can be used during the step of selecting the top few nets (403, Fig. 4) for persistence." '915 Patent at 13:42–43. Step 403 recites, "[s]elect top few nets from ranking" and by ranking it refers to step 402 during which one ranks nets based on unpredictability, i.e., fan-out, and likely QoR impact. *Id.*, Fig. 4. But as Synopsys points out, the patent does not teach a second ranking in step 403. Dkt. No. 118 at 15. Instead, it teaches that "[t]he ranking generated in step 402 can be used to choose the candidate nets that are to be made persistent in step 403." '915 Patent at 7:50–51. The patent recites that during step 403, one can select the top few nets from the ranking in step 700—based on one condition—instead of the ranking in step 402. *See* '915 Patent at 13:42–43. Siemens's construction would therefore improperly exclude this embodiment in the patent. I agree with Synopsys's construction.

V. MOTION TO SEAL

The parties have filed one administrative motion to seal Exhibit 4 of the Joint Claim

Construction and Prehearing Statement. Dkt. No. 101. A party seeking to seal court records must overcome a strong presumption in favor of the public's right to access those records. *See Ctr. for Auto Safety v. Chrysler Grp., LLC*, 809 F.3d 1092, 1096 (9th Cir. 2016), *cert. denied sub nom. FCA U.S. LLC v. Ctr. for Auto Safety*, 137 S. Ct. 38 (2016). In this case, a "good cause" standard applies because claim construction is a nondispositive motion. *Id.* at 1097. "There may be 'good cause' to seal records that are privileged, contain trade secrets, contain confidential research, development or commercial information, or if disclosure of the information might harm a litigant's competitive standing." *See Dugan v. Lloyds TSB Bank, PLC*, No. 12-CV-2549-WHA, 2013 WL 1435223, at *2 (N.D. Cal. Apr. 9, 2013). The language sought to be sealed concerns Synopsys's proprietary, commercially sensitive, and confidential information related to its PrimeTime software, which if made public would cause competitive harm to Synopsys. The motion is therefore GRANTED. Dkt. No. 101.

CONCLUSION

I construe the disputed terms as follows:

Term	Court's Construction
"timing criticality between a pair of registers"	value derived from the data path delay between a pair of registers connected by a data path
"on-chip variations"	process and environmental variations that occur within a chip boundary
"registers [at / in] fixed locations"	registers [at/in] a location that is fixed during clock-tree generation
"Each of said global nets within said second subset routed by one of said threads in isolation of said second subset's other global nets but in respect of the routes of said subset of global nets"	Each global net of the second subset is independently routed by a respective thread, without reference to the routing of any other net within the second subset, and the resulting routing does not conflict with routings of the first subset of global nets
"ranking shorter length and lower fan-out nets over longer length and higher fan-out nets"	Plain and ordinary meaning/no construction necessary
"A multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios"	A database separate from the scenario image that stores a subset of parameter values for a subset of circuit objects in the multiple scenarios

"determin[e/ing . . .] an ECO to fix one or more design requirement violations, wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database"	determin[e/ing . . .] an ECO to fix one or more design requirement violations, wherein said determining includes identifying an ECO to fix a design requirement violation in the scenario and checking that ECO against at least some of the multiple scenarios by estimating parameter values based on parameter values stored in the scenario image and the multi-scenario ECO database
"scenario image"	Information required to detect and/or fix design requirement violations in a circuit design in a particular scenario
"maintains and updates routing" "maintaining [the] existing routes" "maintaining and updating . . . persistent routes" "persistent nets" "persistent global routes"	<u>maintains and updates routing / maintaining and updating . . . persistent routes:</u> updat[es/ing] the routes incrementally as needed to maintain the validity of the route as much as possible <u>maintaining [the] existing routes:</u> leaving routes of persistent nets unchanged <u>persistent nets:</u> nets whose global routes are guaranteed to be preserved as much as possible through subsequent stages <u>persistent global routes:</u> global routes that are guaranteed to be preserved as much as possible through subsequent stages
"ranking [the] nets in a design based on unpredictability and expected quality-of-result impact" "unpredictability and expected quality-of-result impact"	<u>ranking [the] nets in a design based on unpredictability and expected quality-of-result impact:</u> Plain and ordinary meaning/no construction necessary. <u>unpredictability . . . impact:</u> condition where delay misprediction for a net can have a significant impact <u>expected quality-of-result impact:</u> likely timing/electrical criticality

IT IS SO ORDERED.

Dated: September 27, 2021

William H. Orrick
United States District Judge